Small Pad/Small Pitch Dual-Sided Single-Level High-Temp Space Transformer

POSTER #

Prasanna Chitturi/Dominik Schmidt
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Introduction

- As smaller pitch high-density devices come into the marketplace, solutions require that several hurdles need to be overcome – probes, probehead assemblies and the translator interface between the probe card PCB and wafer under test
- Foundry and Logic device manufacturers now have shorter time-to-market requirements and drive the need for quick turnaround in fabrication of custom translators
- With Automotive applications now dominating semiconductor applications, the need for consistent performance at high temperature in rugged conditions is a dominant requirement. This implies a need for a low CTE build that will match CTE of the silicon device.

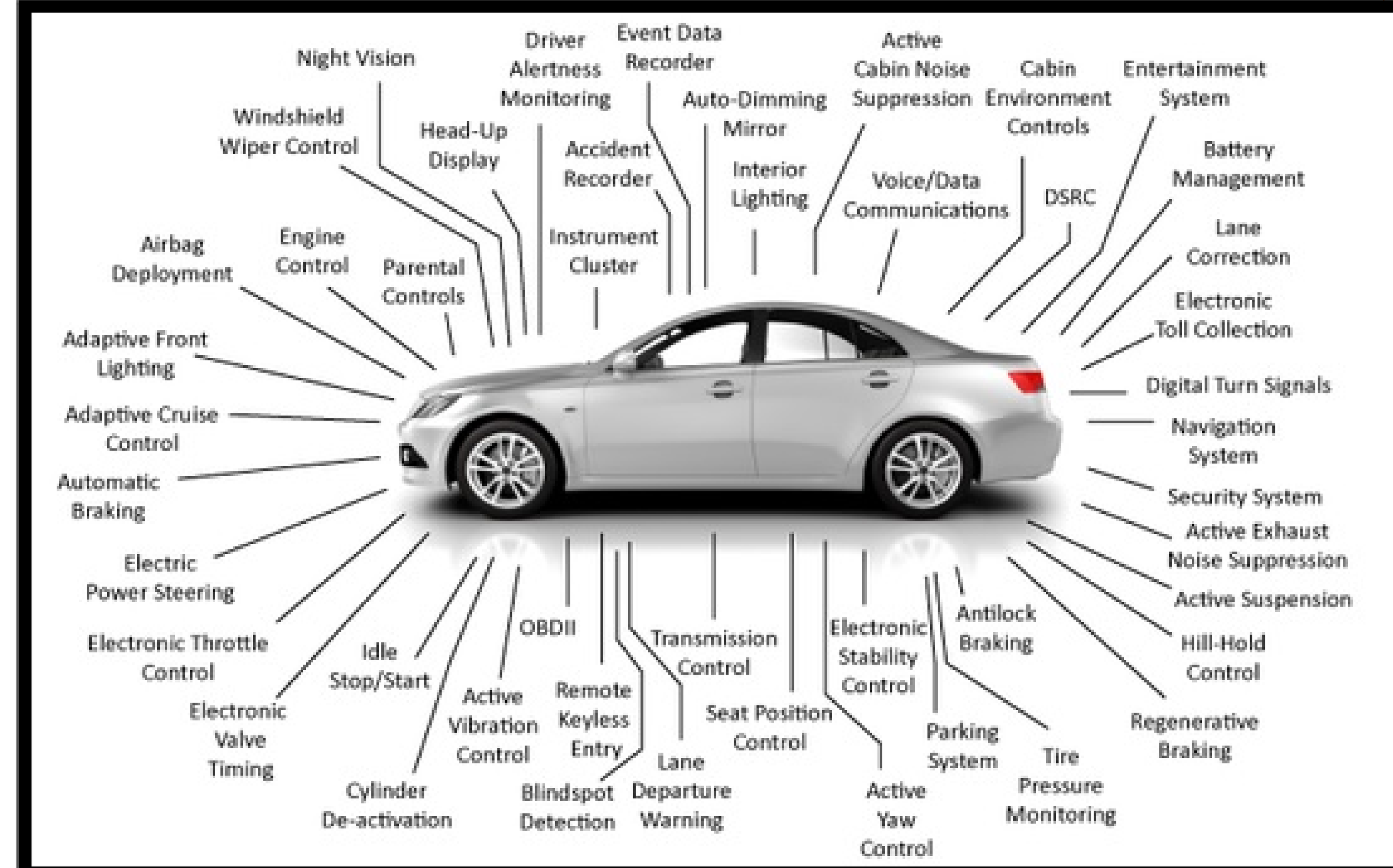


Fig 1 Semiconductor applications in today's automobiles [Power Electronic News - Google]

Solution Requirements

- High Temperature performance
- Low CTE to match that of silicon
- Ruggedized design for durability and reliability
- Fast, repeatable, reliable fabrication process
- Signal/Power integrity
- Minimal crosstalk
- Allow stacking of translators for design latitude

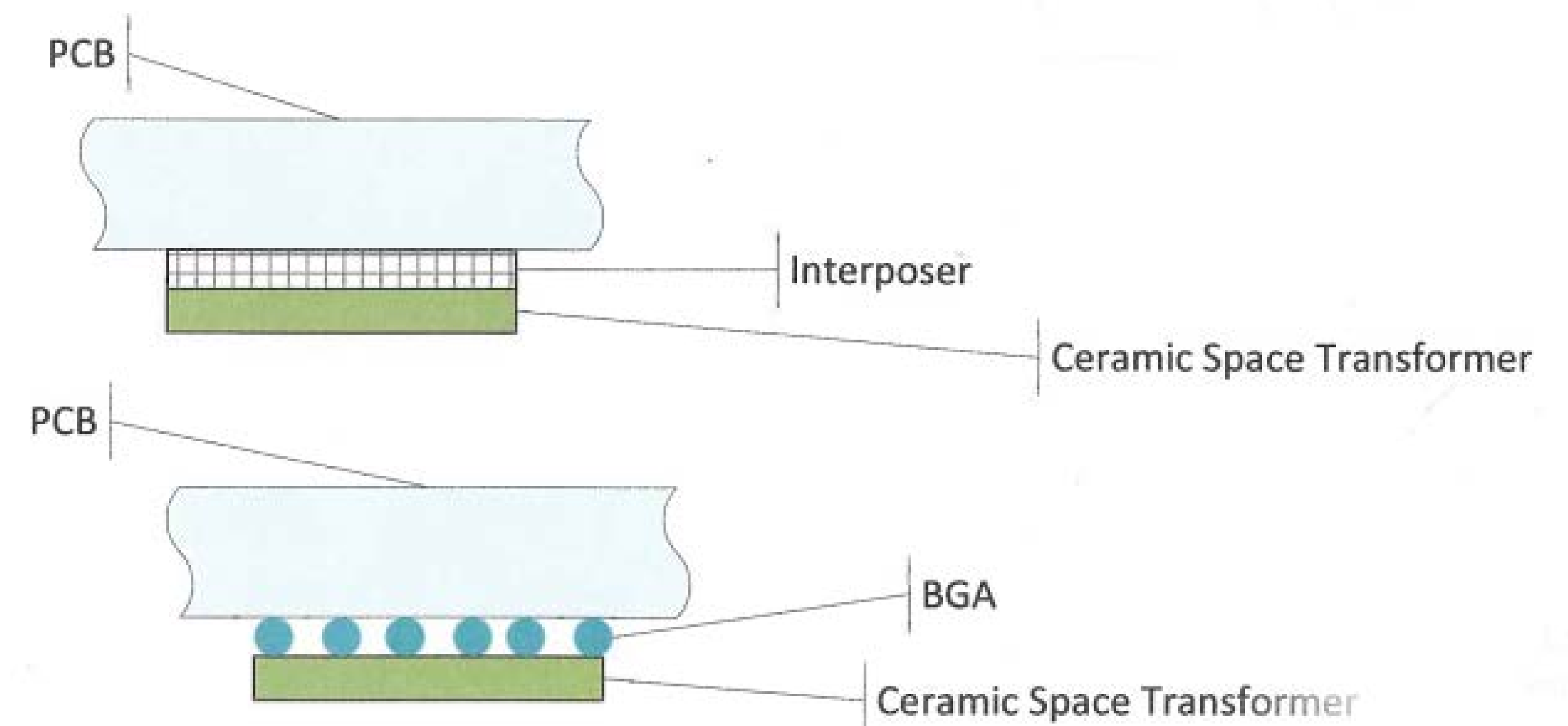
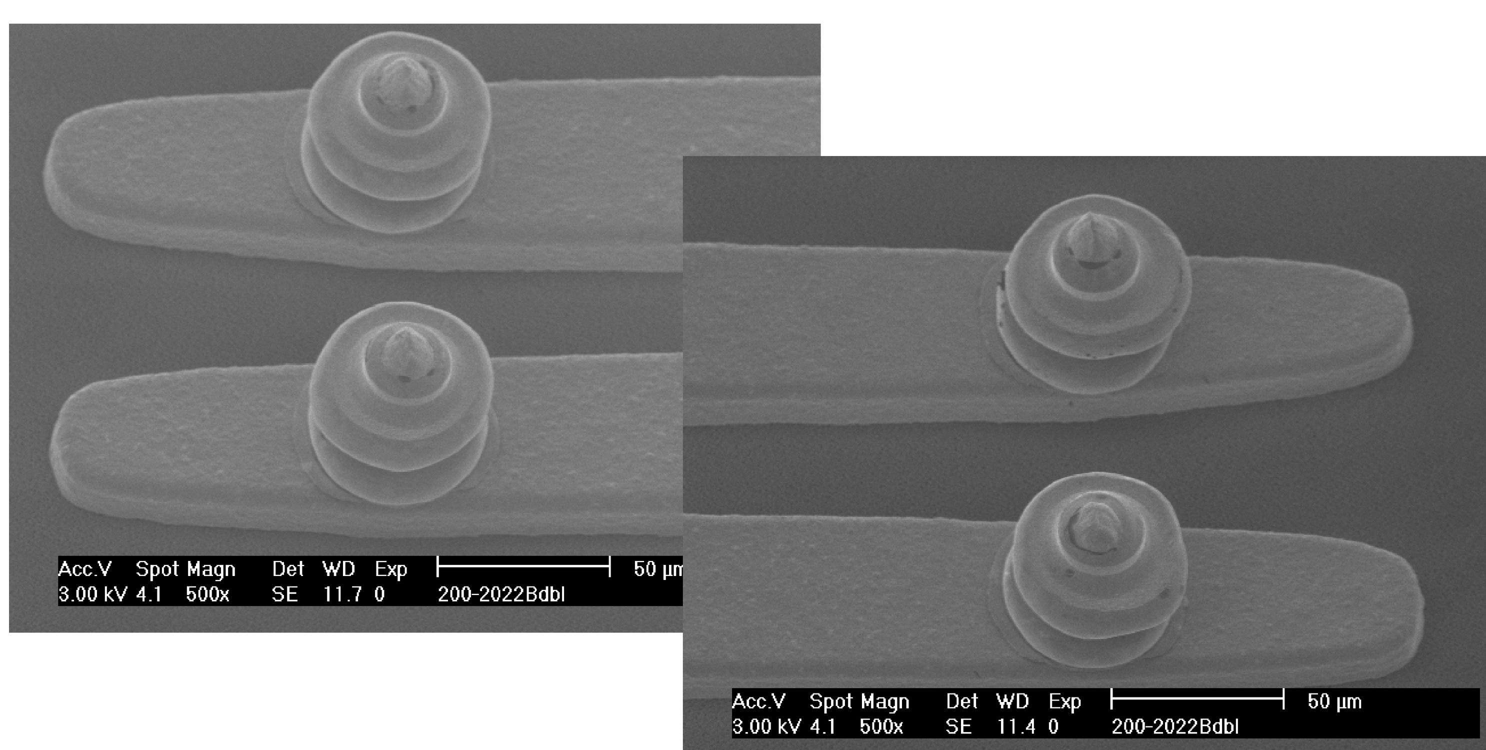
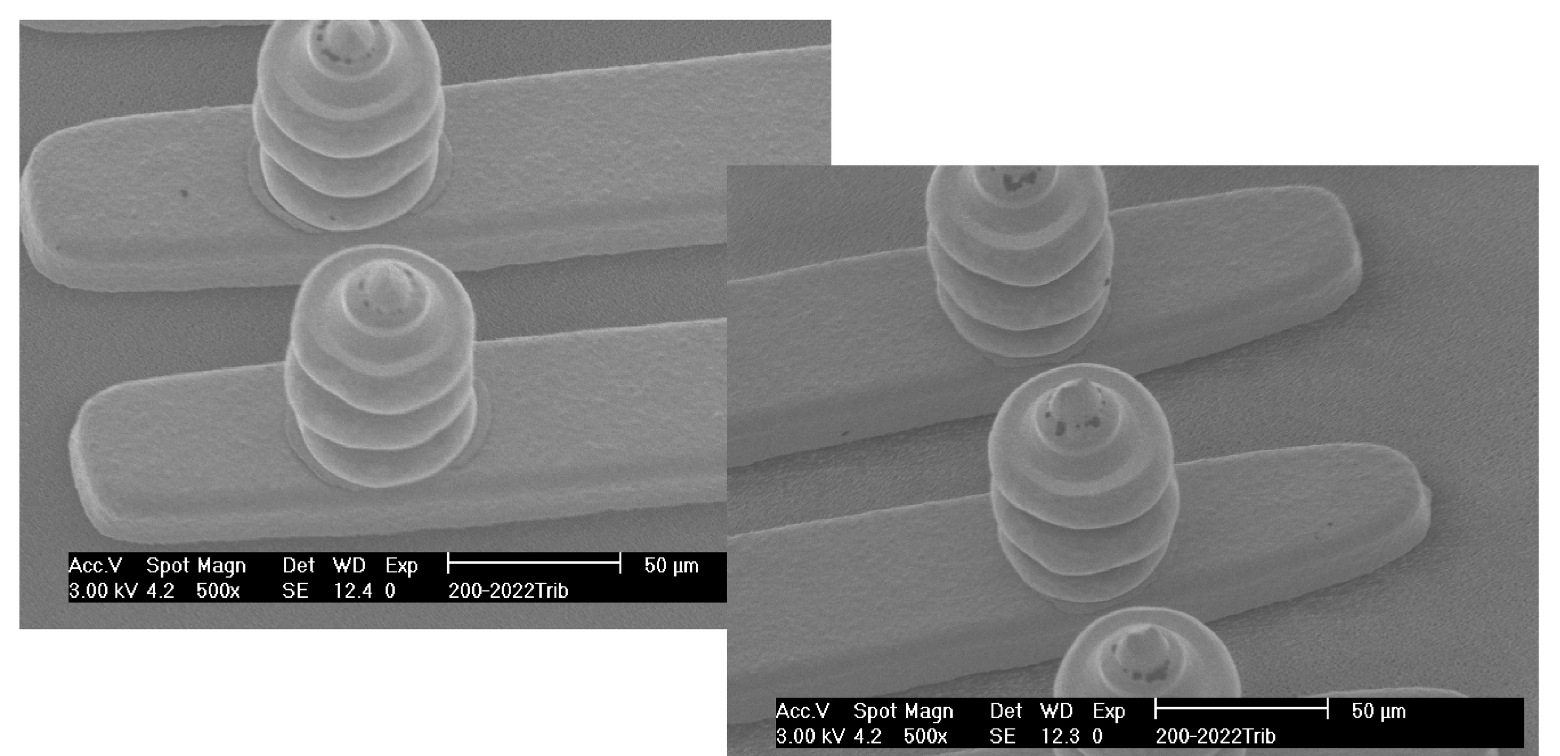


Fig 2 Ceramic space transformer attach to PCB





Double and triple stud bumps for plate stacking – high bond strength of >28gf

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Design Considerations

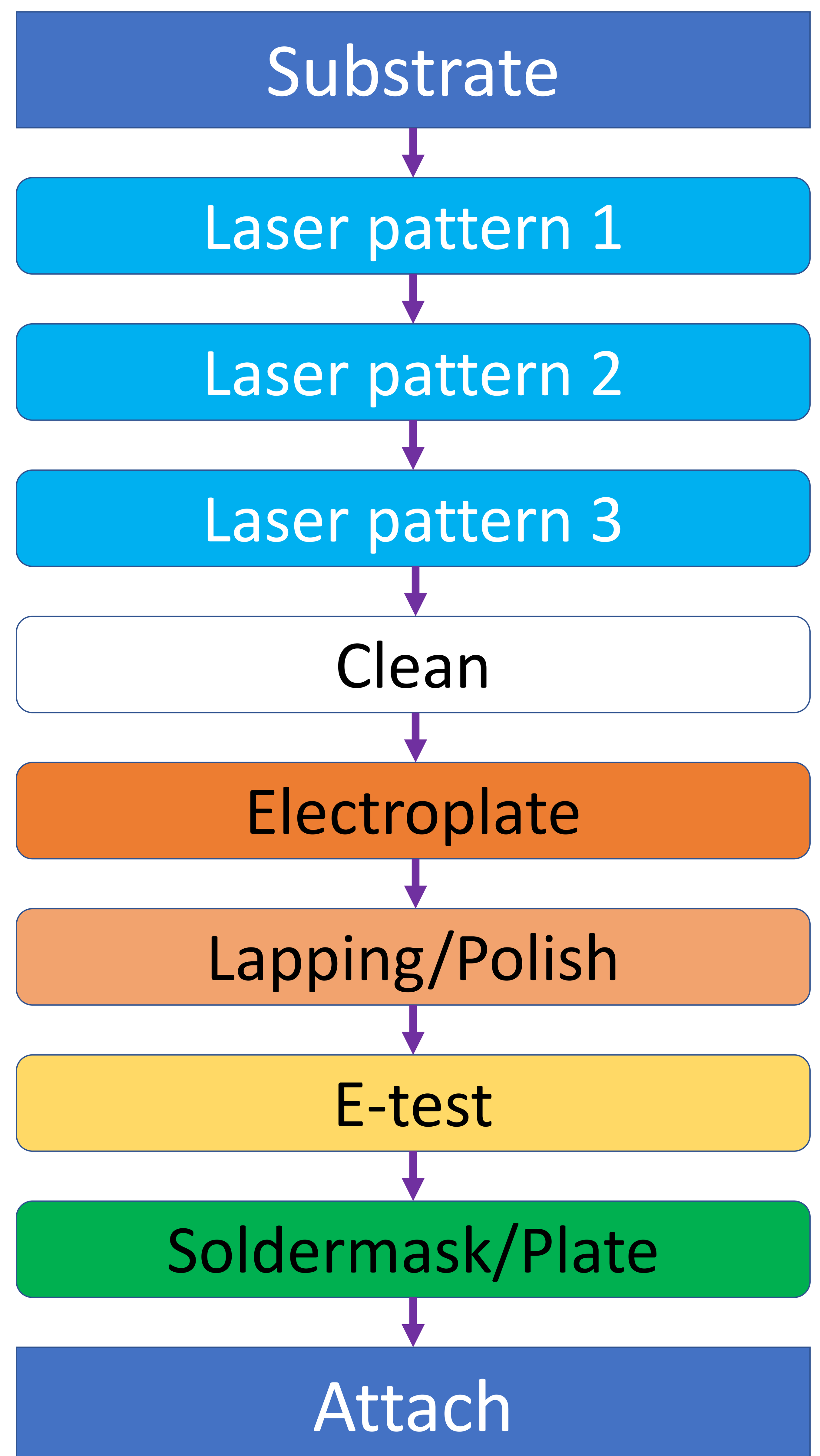
- Varying trace widths to allow for routing around and in between probe pads
- Smallest drawn pitch of 30um
- Smallest via/trench spacing of 10um
- Vias 30um – 30umx50um

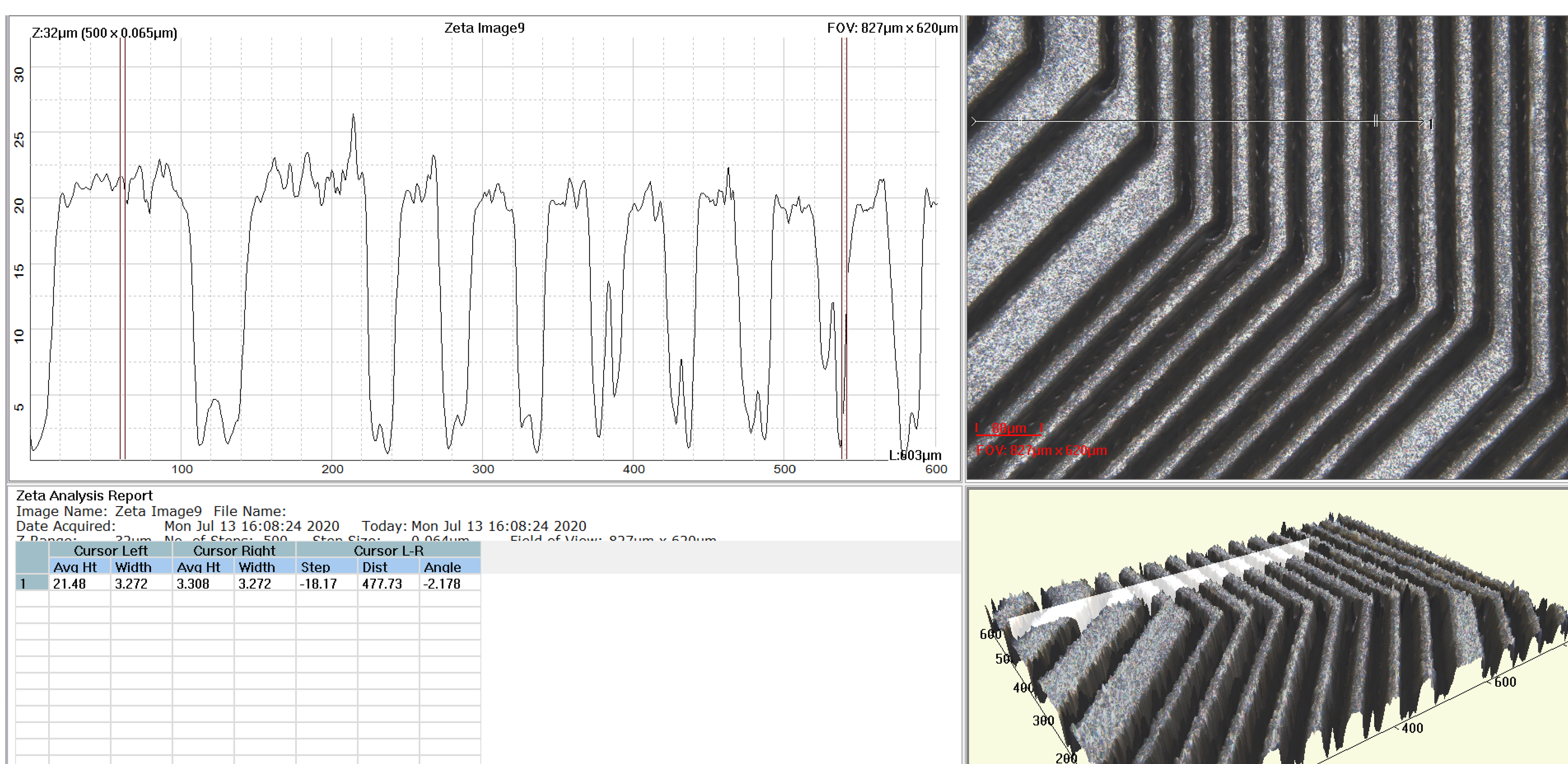
Fabrication – Materials

- High density/high bending strength ceramic with of CTE 2.7 ppm/C
- Vickers hardness of >1200
- High volume resistivity and operating temperatures
- Dk of >8 @10GHz
- Df 0f 25E-4

Fabrication – Methods

- Several approaches of patterning were explored including photolithography and wet and dry etch techniques
- High precision positioning laser milling was chosen as the optimal approach. A combination of laser systems/capabilities were combined to pattern traces, through vias, and pads





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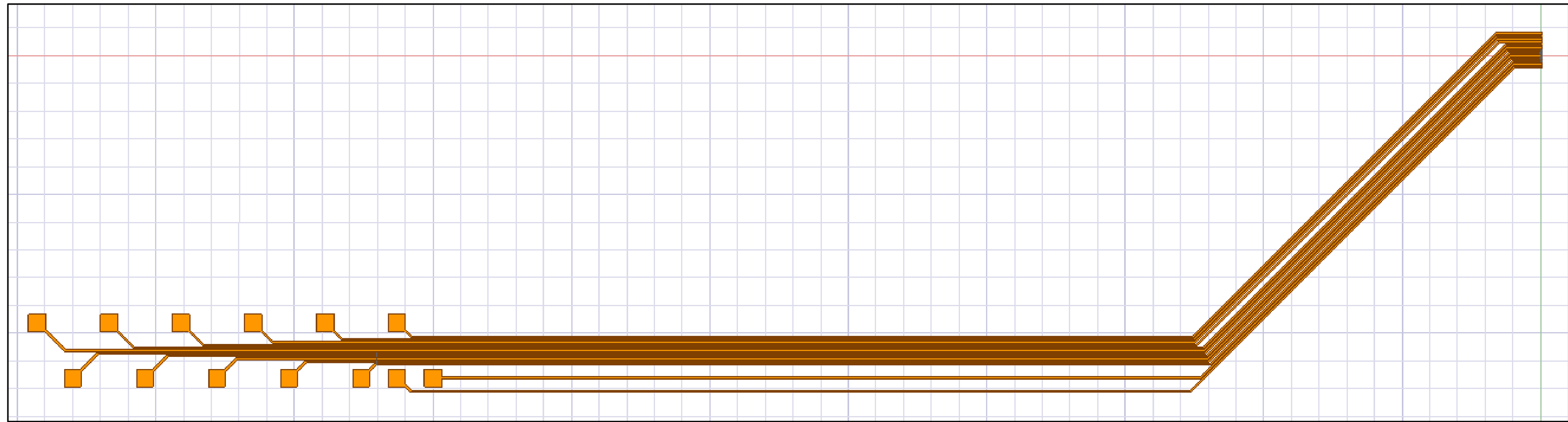
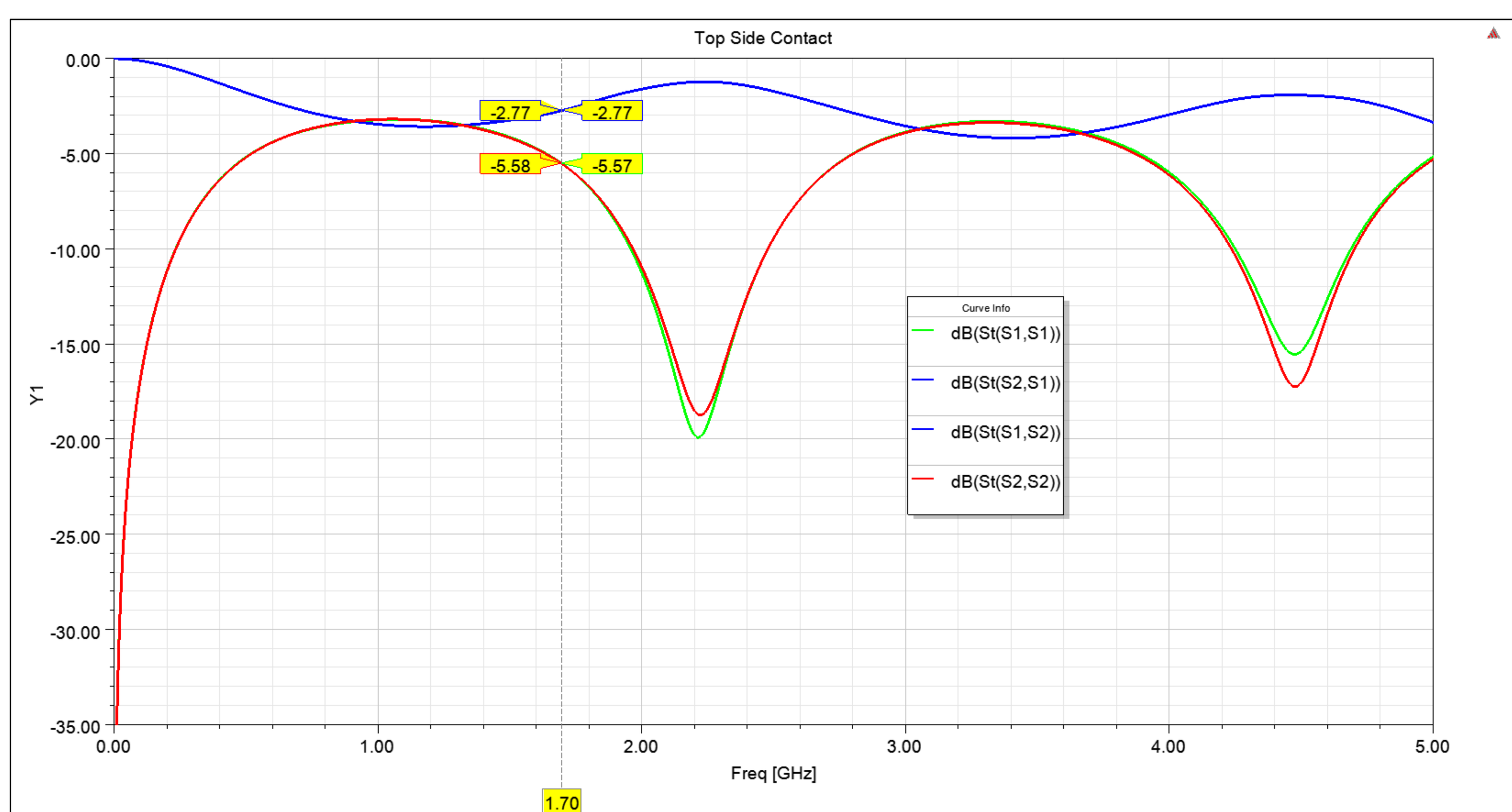
Results

Simulation

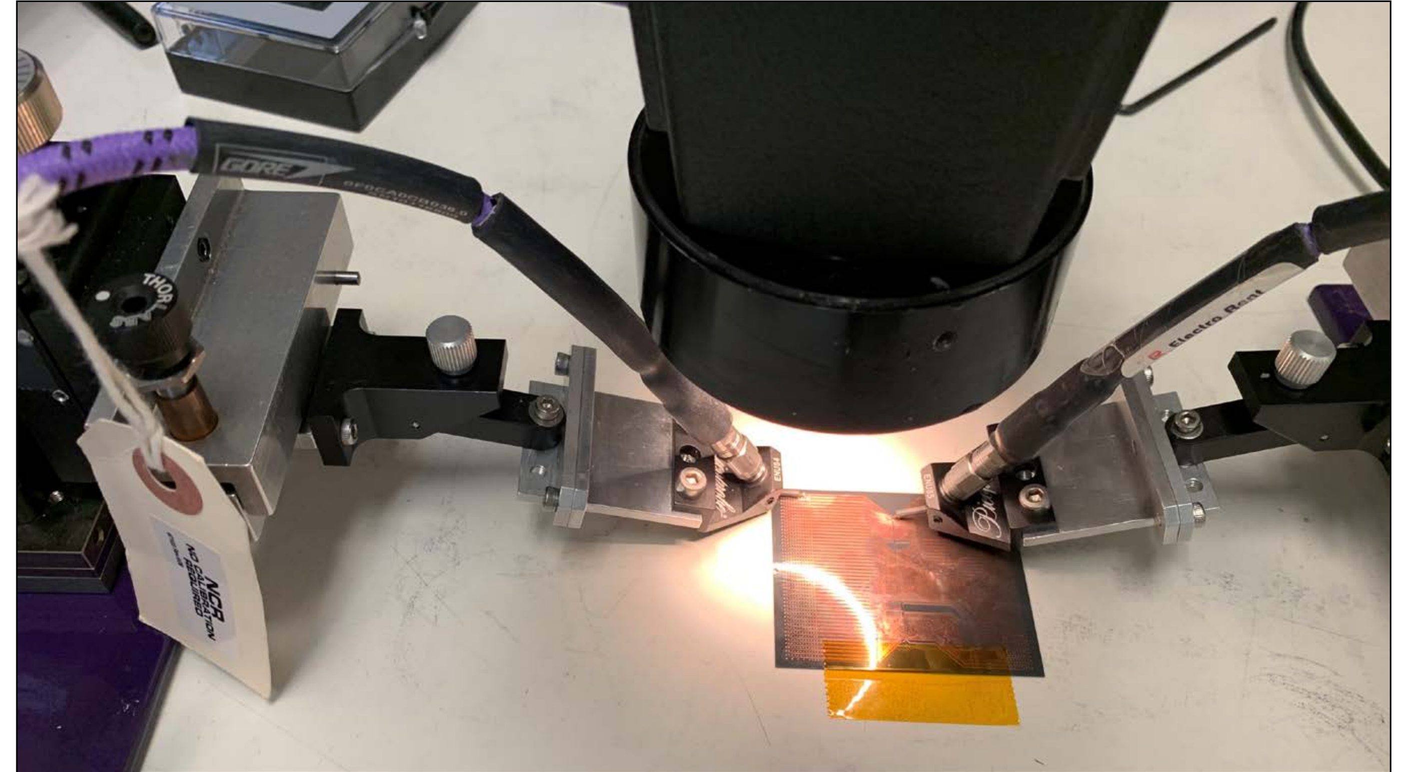


- 2-port measurement on the trace side of board
- Use GSG probes to touch down where traces meet a 50µm pitch at both ends of the trace route
- Although it is not end-to-end path measurement, its response was simulated and compared to the actual measurement

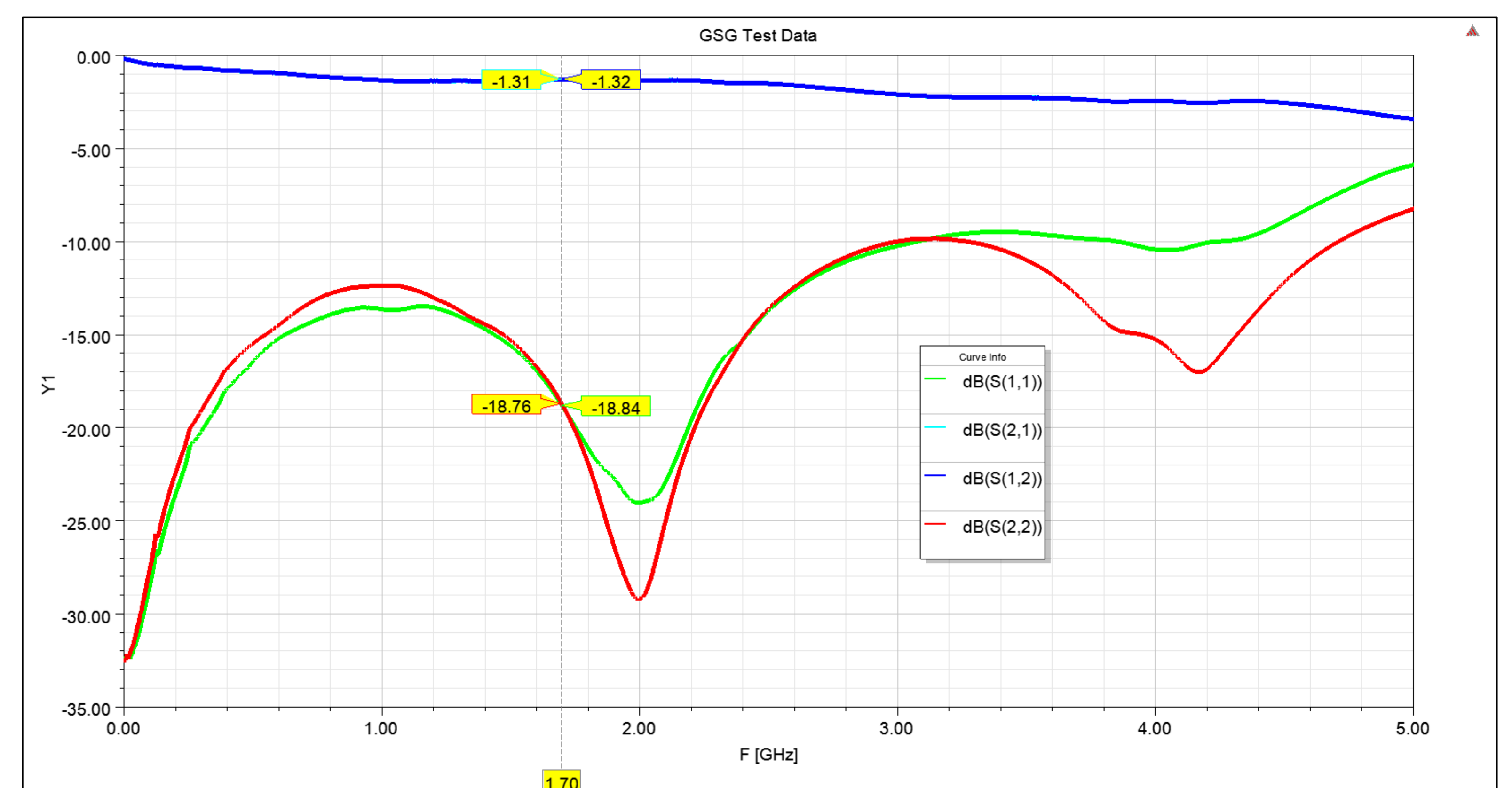


- 2.8 dB insertion loss at 1.7 GHz
- 3dB return loss overall

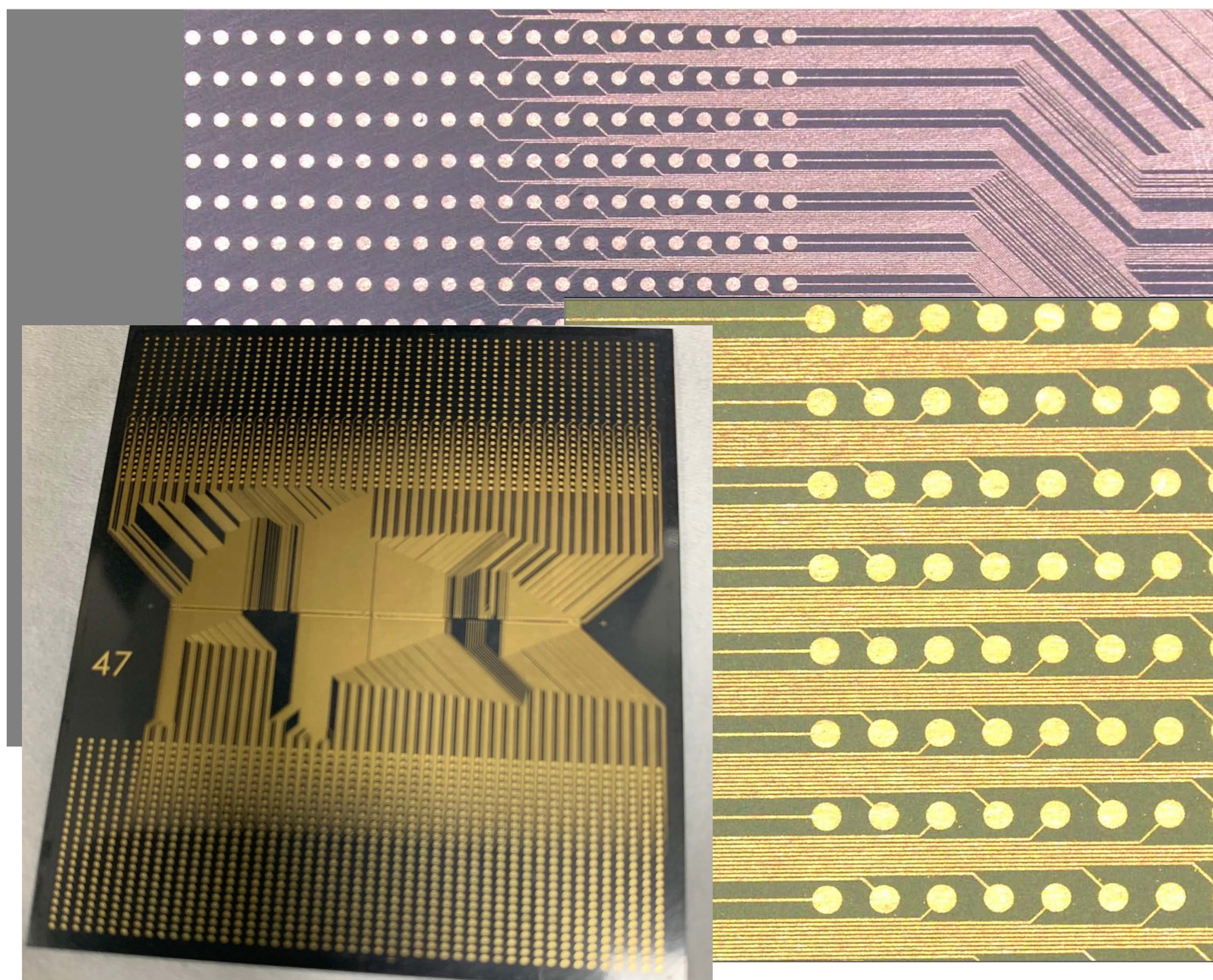
Measurements

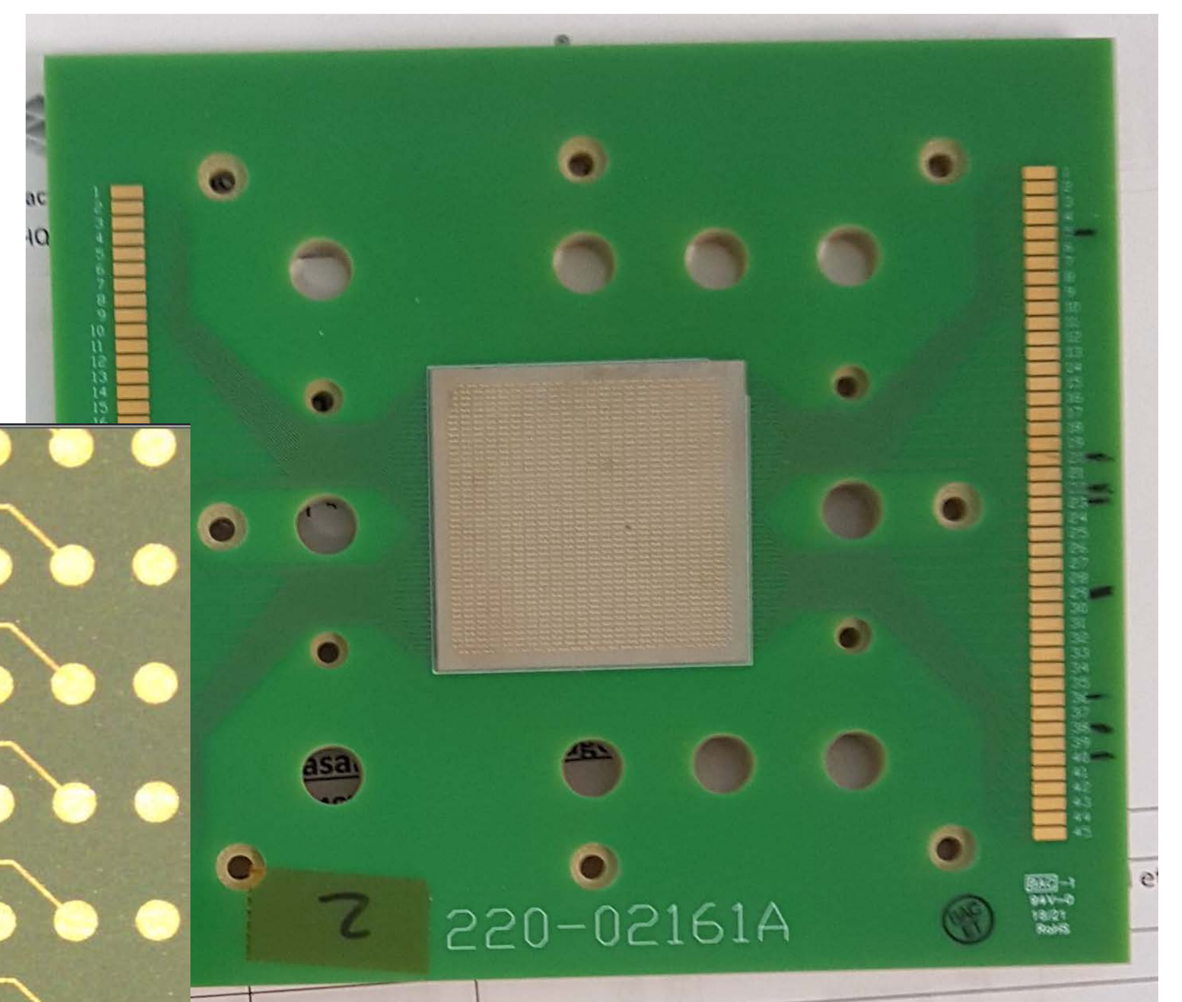


- GSG probe measurement
- DC-5GHz measurement



- 1.3 dB insertion loss at 1.7 GHz
- >10 dB return loss at <3 GHz





BGA attached

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